CLAIMS

1. A digital phase locked loop circuit for generating sampling clock signals used with respect to a plurality of channels for sampling reproduced information simultaneously from a plurality of tracks of a recording medium, comprising:

an average frequency computing circuit for calculating an average frequency of the phase locked sampling clock signals in selected channels and feeding back the calculated average to the phase locked loop;

wherein the average frequency computing circuit outputs a frequency error signal with respect to any channel in which the frequency of the sampling clock signals is outside an allowable frequency range.

2. The digital phase locked loop circuit according to Claim 1, wherein the average frequency computing circuit comprises a comparator for comparing the frequency of the sampling clock signals in each channel with the allowable frequency range and for outputting a frequency error signal for any channel in which the frequency of the sampling clock signals is outside an allowable frequency range.

3. The digital phase locked loop circuit according to Claim 2, wherein the average frequency computing circuit calculates the average frequency of the sampling clock signals in the selected channels which do not include those channels in which the

frequency of the sampling clock signals is outside the allowable frequency range.

4. The digital phase locked loop circuit according to Claim 2, further comprising:

a register for adjustably setting a value representative of an allowable deviation,

wherein the allowable frequency range is determined on the basis of the average frequency calculated by the average frequency computing circuit and the set value from the register.

5. The digital phase locked loop circuit according to Claim 2, further comprising a gate circuit for masking the frequency error signal in an operational mode other than a tracking mode.

6. The digital phase locked loop circuit, according to Claim 2, wherein the average frequency computing circuit divides the plurality of channels into a plurality of groups each of which includes at least two channels, the frequencies of the sampling clock signals for the plurality of channels being summed repetitively and cumulatively group by group for calculating the average frenquency.

7. The digital phase locked loop circuit according to Claim 2, wherein the average frequency computing circuit is reset in a calibration mode for performing calibration of the frequencies to be phase locked.

8. The digital phase locked loop circuit according to Claim 2, wherein the average frequency computing circuit includes a holding circuit for holding the average frequency which has been obtained immediately previously when all of the channels are in an operational mode other than a tracking mode.

9. The digital phase locked loop circuit according to Claim 2, wherein when the average frequency computing circuit outputs a frequency error signal for any channel, resynchronization of the sampling clock signals is performed only for the erring channel.

10. The digital phase locked loop circuit according to Claim 9, wherein the resynchronization of the sampling clock signals is performed at high speed in a lead-in mode by using the average frequency calculated by the average frequency computing circuit.

11. A digital phase locked loop circuit for generating sampling clock signals used with respect to a plurality of channels for sampling reproduced information simultaneously from a plurality of tracks of a recording medium, comprising:

an average frequency computing circuit for calculating an average frequency of the phase locked sampling clock signals in selected channels and feeding back the calculated average to the phase locked loop;

wherein the average frequency computing circuit comprises a speed variation detecting circuit for determining a rate of variation of the average frequency in a predetermined time.

12. The digital phase locked loop circuit according to Claim 11, wherein the rate variation detecting circuit includes a comparator for comparing a variation width, in the predetermined time, of the average frequency determined by the average frequency computing circuit with an allowable variation range and for outputting a speed error signal if the variation width is outside the allowable variation range.

13. The digital phase locked loop circuit according to Claim 11, wherein the speed variation detecting circuit is capable of adjustably setting the predetermined time.